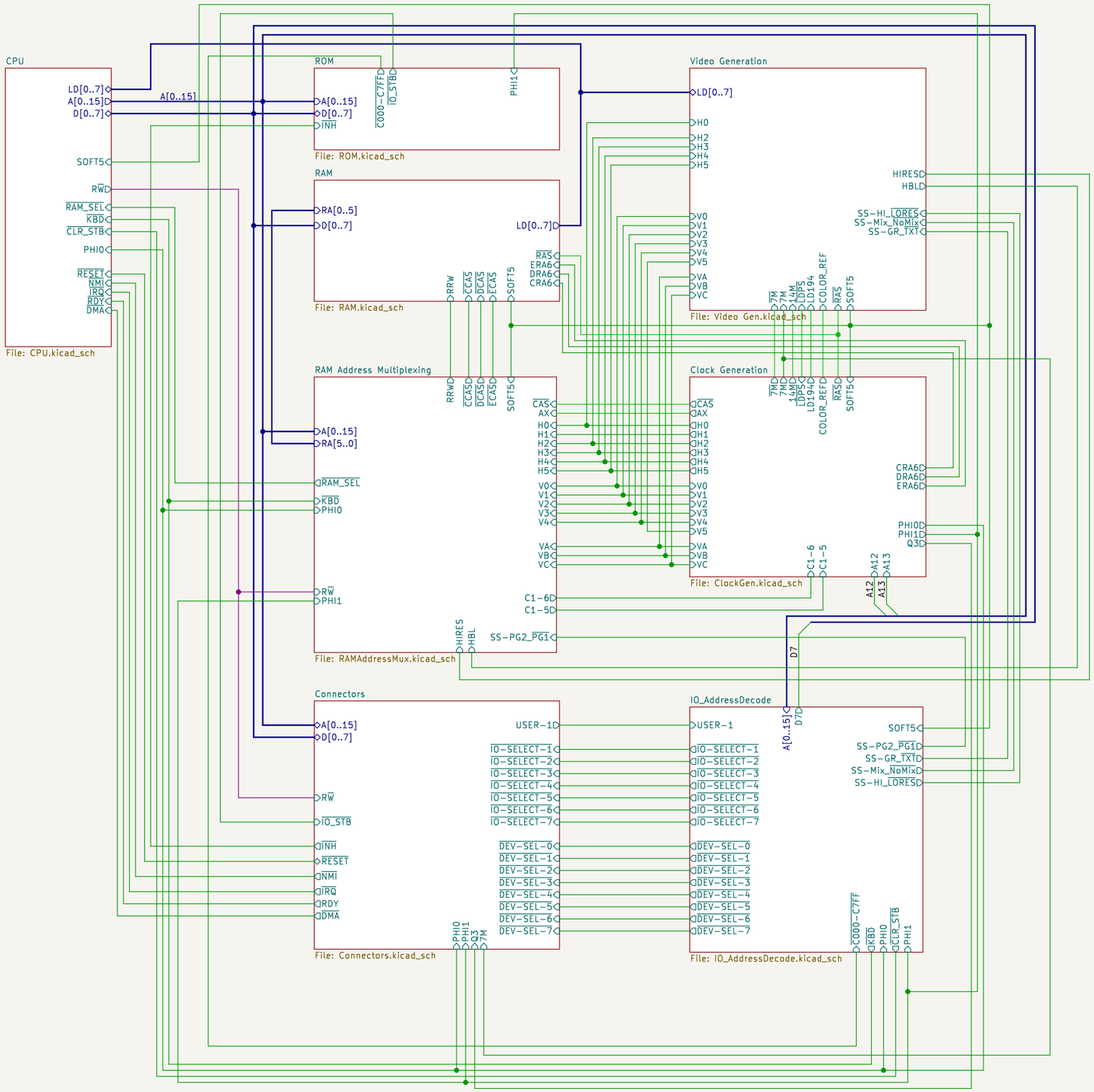
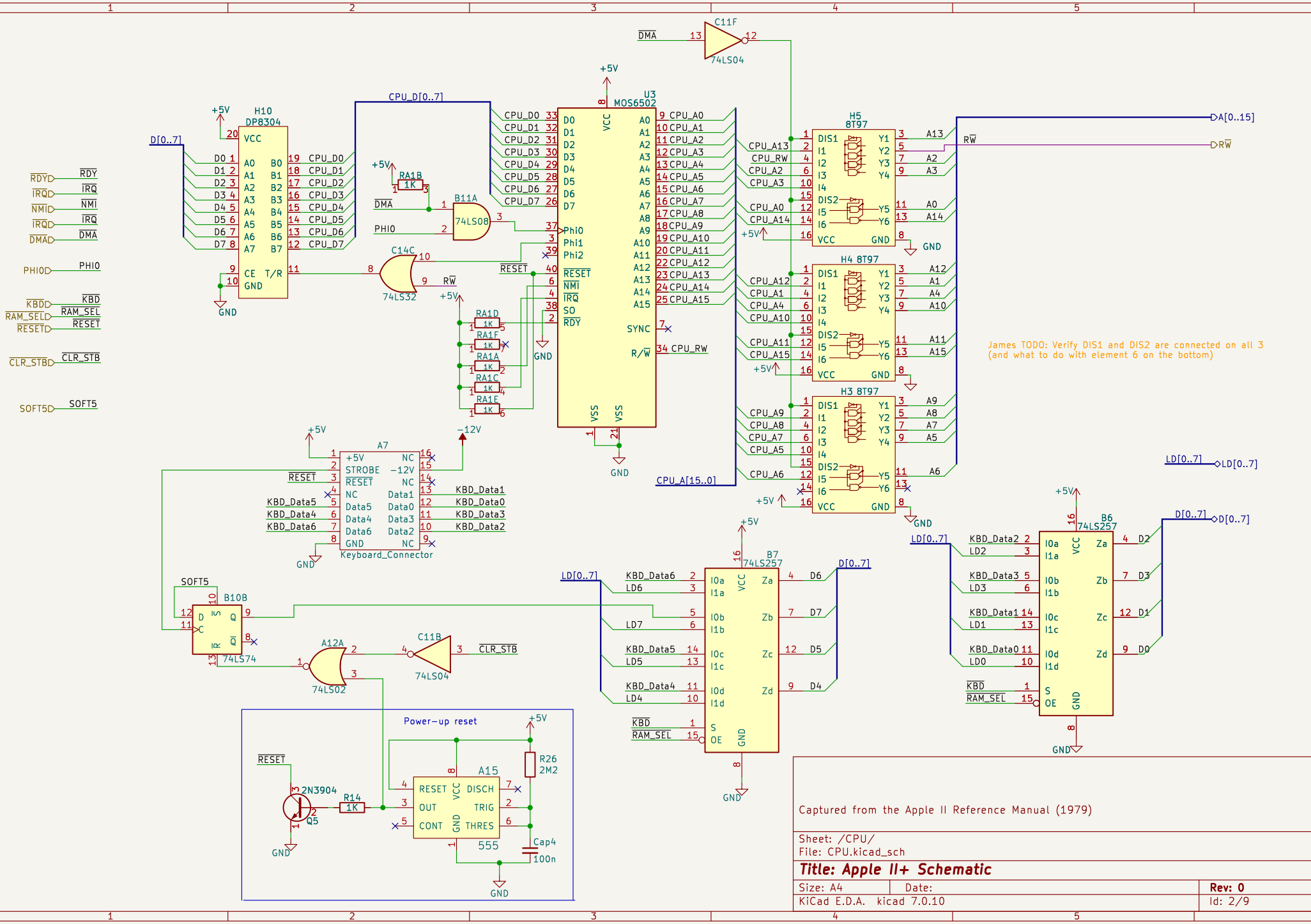


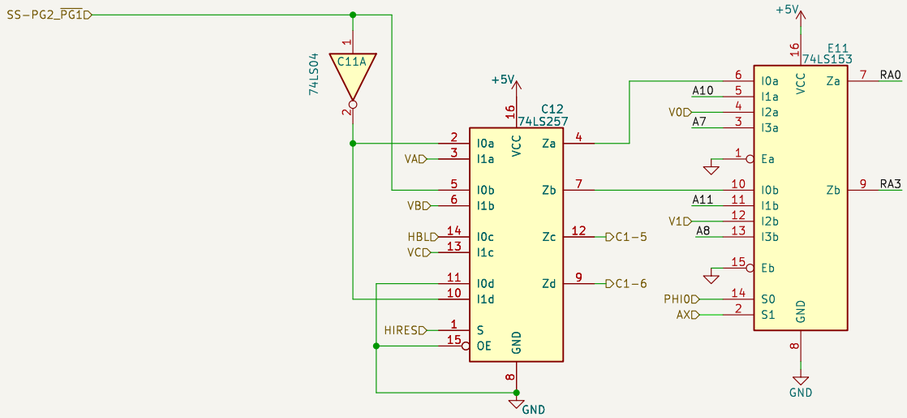
Captured from the Apple II Reference Manual (1979)

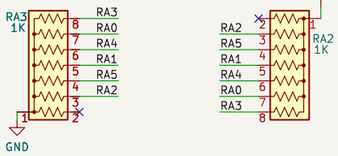
Sheet: /
File: AppleII+.kicad_sch

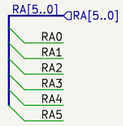
Title: Apple II+ Schematic

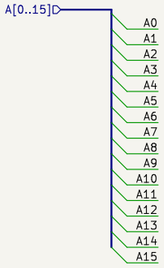
Size: A3	Date:	**Rev: 0**
KiCad E.D.A. kicad 7.0.10		Id: 1/9

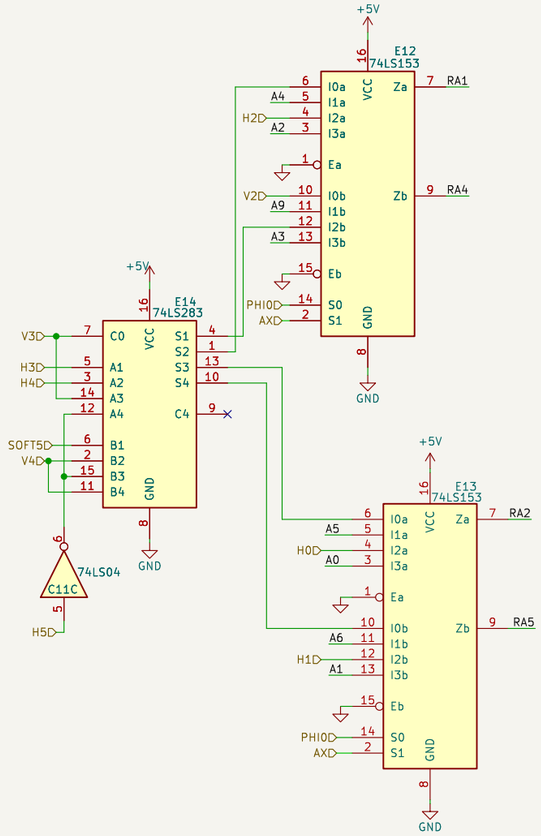

RDY
IRQ
NMI
IRQ
DMA
PHI0
KBD
RAM_SEL
RESET
CLR_STB
SOFT5
H10
DP8304
D[0..7]
CPU_D[0..7]
U3
MOS6502
C11F
74LS04
DMA
RA1B
1K
B11A
74LS08
PHI0
C14C
74LS32
RW
RESET
RA1D
RA1F
RA1A
RA1C
RA1E
A7
Keyboard_Connector
KBD_Data1
KBD_Data0
KBD_Data3
KBD_Data2
KBD_Data5
KBD_Data4
KBD_Data6
B10B
74LS74
A12A
74LS02
C11B
CLR_STB
B7
74LS257
LD[0..7]
D[0..7]
B6
H5
8T97
H4 8T97
H3 8T97
CPU_A[15..0]
A[0..15]
James TODO: Verify DIS1 and DIS2 are connected on all 3
(and what to do with element 6 on the bottom)
Power-up reset
A15
555
R26
2M2
R14
2N3904
Q5
Cap4
100n
Captured from the Apple II Reference Manual (1979)
Sheet: /CPU/
File: CPU.kicad_sch
Title: Apple II+ Schematic
Size: A4
Date:
Rev: 0
KiCad E.D.A. kicad 7.0.10
Id: 2/9

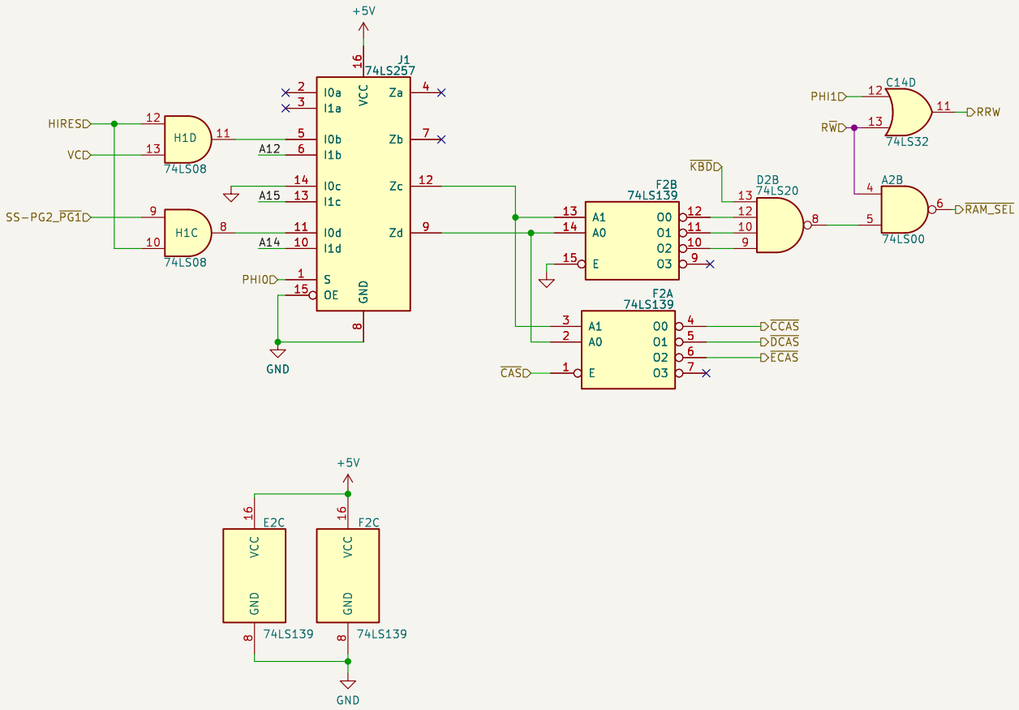










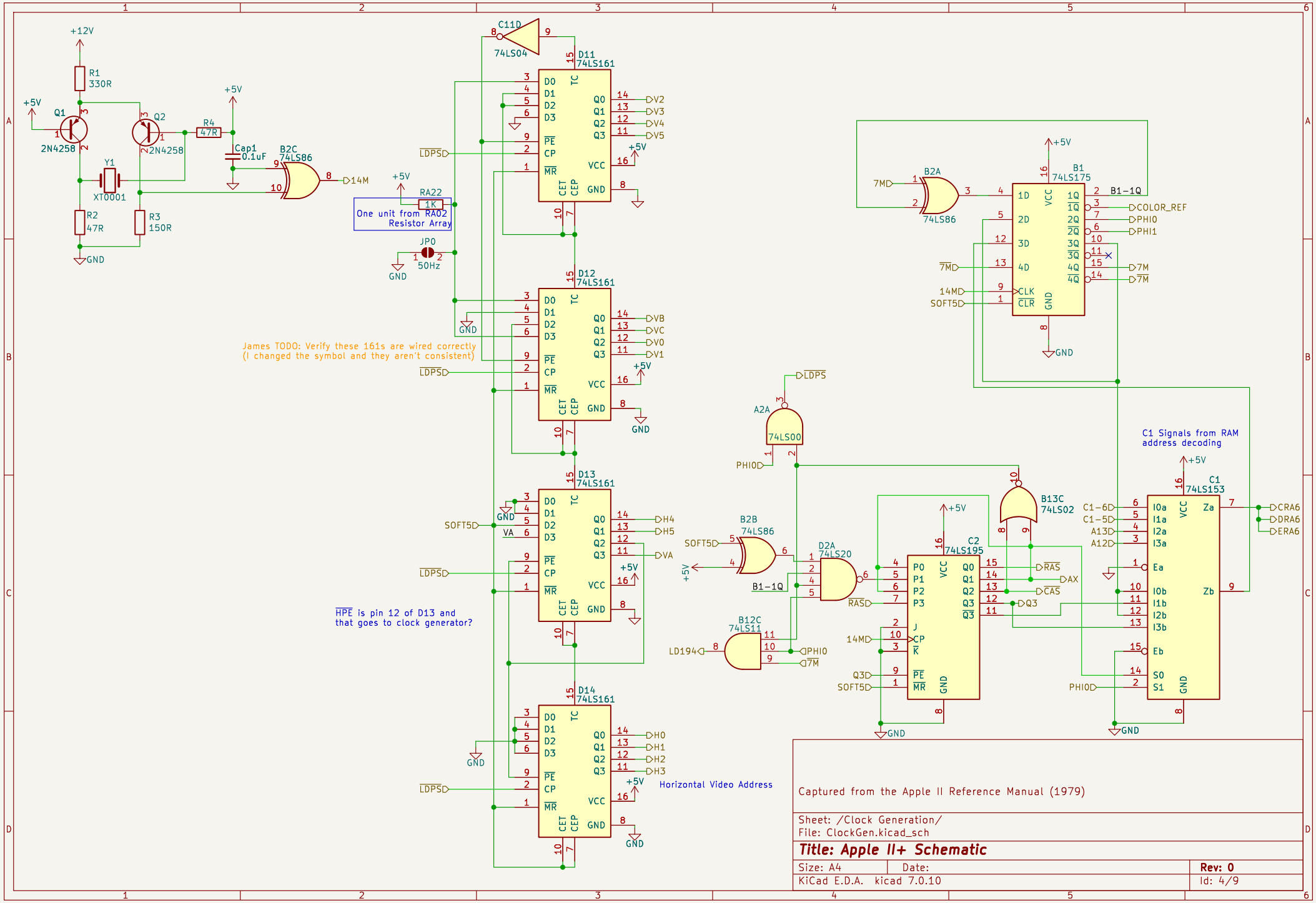


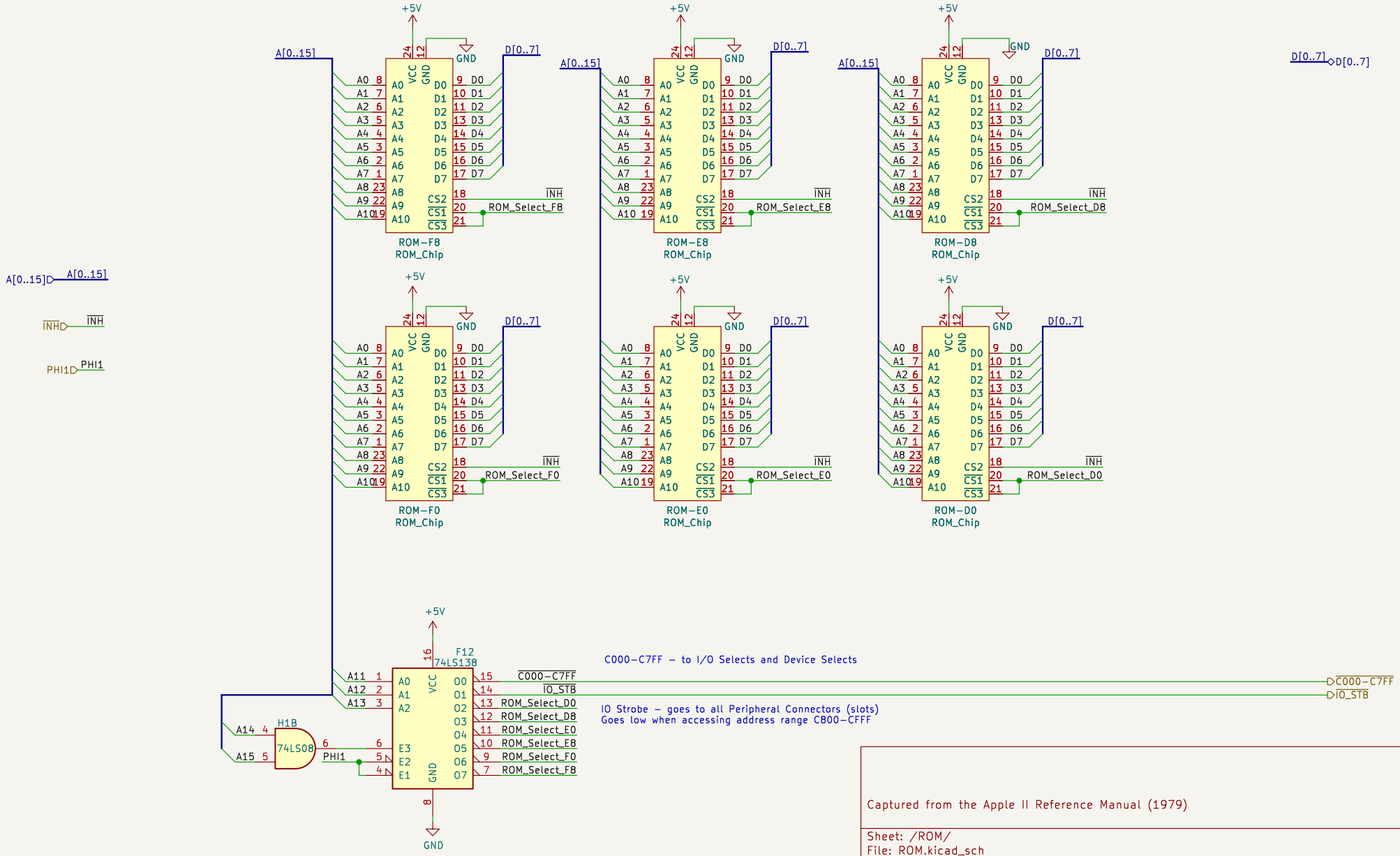
Captured from the Apple II Reference Manual (1979)

Sheet: /RAM Address Multiplexing/
File: RAMAddressMux.kicad_sch

Title: Apple II+ Schematic

Size: A3	Date:	**Rev: 0**
KiCad E.D.A. kicad 7.0.10		Id: 3/9


+12V
R1
330R
+5V
Q1
2N4258
Q2
2N4258
R4
47R
Cap1
0.1uF
Y1
XT0001
R2
47R
R3
150R
GND
B2C
74LS86
14M
C11D
74LS04
D11
74LS161
D12
74LS161
D13
74LS161
D14
74LS161
LDPS
RA22
1K
One unit from RA02
Resistor Array
JP0
50Hz
V2
V3
V4
V5
VB
VC
V0
V1
H4
H5
VA
H0
H1
H2
H3
SOFT5
James TODO: Verify these 161s are wired correctly
(I changed the symbol and they aren't consistent)
HPE is pin 12 of D13 and
that goes to clock generator?
Horizontal Video Address
B2A
74LS86
7MD
B1
74LS175
B1-1Q
COLOR_REF
PHI0
PHI1
7M
14MD
SOFT5
A2A
74LS00
PHI0D
B2B
74LS86
B12C
74LS11
LD194
D2A
74LS20
B1-1Q
RAS
B13C
74LS02
C2
74LS195
AX
CAS
Q3
14MD
C1 Signals from RAM
address decoding
C1
74LS153
C1-6D
C1-5D
A13
A12
CRA6
DRA6
ERA6
Captured from the Apple II Reference Manual (1979)
Sheet: /Clock Generation/
File: ClockGen.kicad_sch
Title: Apple II+ Schematic
Size: A4
Date:
Rev: 0
KiCad E.D.A. kicad 7.0.10
Id: 4/9


A[0..15]
D[0..7]
INH
PHI1
+5V
GND
ROM-F8
ROM_Chip
ROM_Select_F8
ROM-E8
ROM_Select_E8
ROM-D8
ROM_Select_D8
ROM-F0
ROM_Select_F0
ROM-E0
ROM_Select_E0
ROM-D0
ROM_Select_D0
F12
74LS138
H1B
74LS08
C000-C7FF
IO_STB
C000-C7FF – to I/O Selects and Device Selects
IO Strobe – goes to all Peripheral Connectors (slots)
Goes low when accessing address range C800-CFFF
Captured from the Apple II Reference Manual (1979)
Sheet: /ROM/
File: ROM.kicad_sch
Title: Apple II+ Schematic
Size: A4
Date:
Rev: 0
KiCad E.D.A. kicad 7.0.10
Id: 5/9

RA[0..5]
CRA6
DRA6
ERA6
CCAS
DCAS
ECAS
RAS
RRW
D[0..7]
D0
D1
D2
D3
D4
D5
D6
D7
SOFT5

E3 4116 −5V +12V +5V
E4 4116 −5V +12V +5V
E5 4116 −5V +12V +5V
E6 4116 −5V +12V +5V
E7 4116 −5V +12V +5V
E8 4116 −5V +12V +5V
E9 4116 −5V +12V +5V
E10 4116 −5V +12V +5V

RA0 10
RA1 11
RA2 12
RA3 7
RA4 6
RA5 5
ERA6 13
ECAS 15
RAS 4
RRW 3
A0 A1 A2 A3 A4 A5 A6
VBB 1
VDD 8
VCC 9
CAS RAS RW
DO 14
DI 2
GND 16

RDO0 RDO1 RDO2 RDO3 RDO4 RDO5 RDO6 RDO7
D0 D1 D2 D3 D4 D5 D6 D7

D3 4116 −5V +12V +5V
D4 4116 −5V +12V +5V
D5 4116 −5V +12V +5V
D6 4116 −5V +12V +5V
D7 4116 −5V +12V +5V
D8 4116 −5V +12V +5V
D9 4116 −5V +12V +5V
D10 4116 −5V +12V +5V

DRA6 13
DCAS 15

C3 4116 −5V +12V +5V
C4 4116 −5V +12V +5V
C5 4116 −5V +12V +5V
C6 4116 −5V +12V +5V
C7 4116 −5V +12V +5V
C8 4116 −5V +12V +5V
C9 4116 −5V +12V +5V
C10 4116 −5V +12V +5V

CRA6 13
CCAS 15

B50 74LS174
B80 74LS174

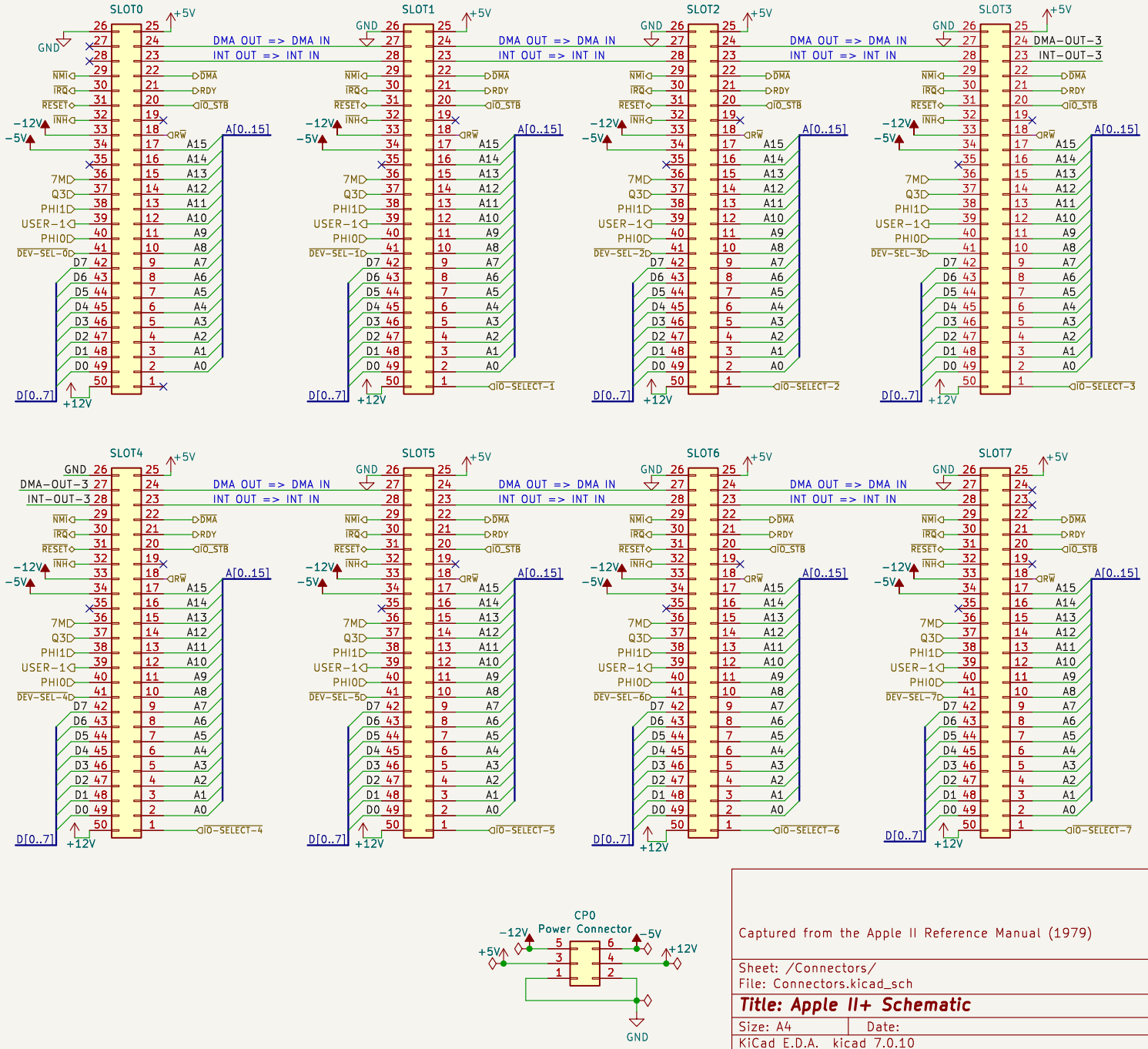
D0 D1 D2 D3 D4 D5 Q0 Q1 Q2 Q3 Q4 Q5
Cp Mr VCC GND

RDO2 RDO3 RDO0 RDO1 RDO6 RDO7 RDO4 RDO5
LD2 LD3 LD0 LD1 LD6 LD7 LD4 LD5
LD[0..7]

LD0..7 = Latched Data bus
feeding Video Generator sections

Captured from the Apple II Reference Manual (1979)

Sheet: /RAM/ File: RAM.kicad_sch	
Title: Apple II+ Schematic	
Size: A3 | Date:	**Rev: 0**
KiCad E.D.A. kicad 7.0.10	Id: 6/9



Captured from the Apple II Reference Manual (1979)

Sheet: /Connectors/
File: Connectors.kicad_sch

Title: Apple II+ Schematic

Size: A4	Date:	Rev: 0
KiCad E.D.A. kicad 7.0.10		Id: 7/9

Why isn't there an H1 here?

VA VB VC V0 V2 V1 V5 H4 H5 H3 H2 H0 COLOR_REF

74LS02 74LS04 74LS08 74LS11 74LS32 74LS00 74LS74 74LS86 74LS151 74LS166 74LS194 74LS257 74LS174

JP14 JP16 JP12 JP13 JP11 JP10 JP9 50Hz 60Hz

C11E C13A C13B C14B B14A B14B B14C B14D B11C B11D B11A B11B A12B A12C A12D B12A B12B B12D B13A B13B B13D A2C A2D B5A B8F B8A A11A A11B A12-13 C14-6 HBL HIRES Text_Video

R5 1K R7 1K5 R8 2K R6 2K7 R9 10R R10 27R L7 L R11 200R R12 12K R13 3K3 R27 4K7 C15 100n Cap2 47pf CT3 5-50pf L1 27uH Cap14 100n Cap13 100n

Q3 2N3904 Q6 2N3904

+5V +12V -5V GND

J18 Aux Video

TP1 Wire wrap post

K14 VIDEO OUT

VIDEO_DATA SYNC Color_Burst SS-GR_TXT

LD[0..7] LD7 LD6 LD5 LD4 LD3 LD2 LD1 LD0

CHAR-ROM17 2316_2716

555 B3 RESET VCC OUT DISCH THRES TRIG GND

Flashing timer for flashing chars

A3 74LS166 A3-1 A3-2

A5 A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7 VCC VDD

A9 74LS151 A12-13

A10 74LS194 A8-3-A9-B9 B9-13

B4 74LS194 B9 74LS194

A8 74LS257

SOFT5 LDPS 14M 7M LD194 RAS SS-GR_TXT SS-Mix_NoMix SS-HI_LORES

SS-HI_LORES

Exclude DRC error about Output and Output on A2 8 and 11 because they will never go low.

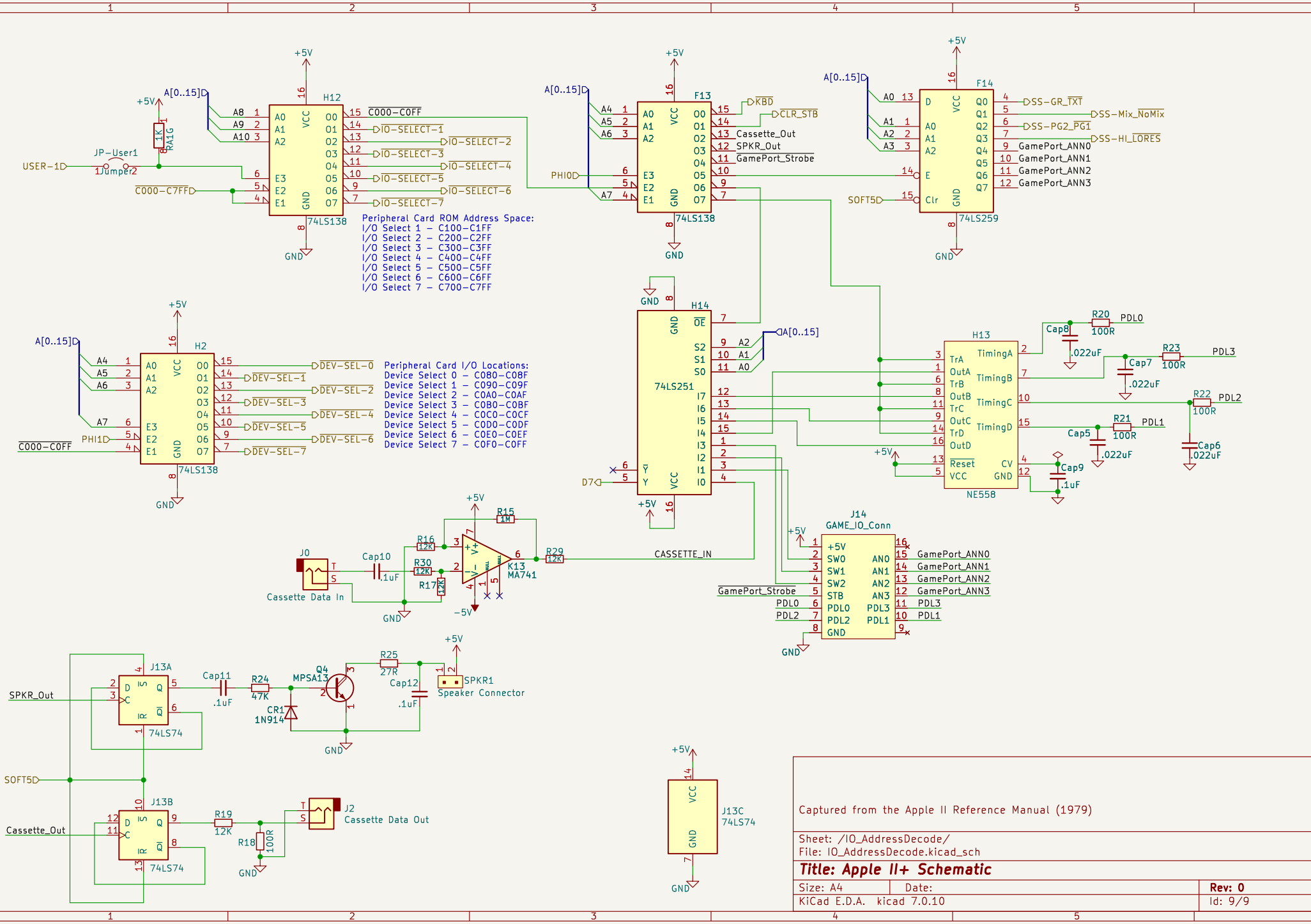
From "The Apple II Circuit Description", page 152:
Soft S-Rev.7 and earlier boards use high outputs of gates A2-8 and A2-11 instead of R28 to pull up unused logic inputs

Captured from the Apple II Reference Manual (1979)

Sheet: /Video Generation/
File: Video Gen.kicad_sch

Title: Apple II+ Schematic

Size: A3	Date:	Rev: 0
KiCad E.D.A. kicad 7.0.10		Id: 8/9


H12
74LS138
A[0..15]
+5V
GND
JP-User1
Jumper2
USER-1
RA1G
1K
C000-C7FF
C000-C0FF
IO-SELECT-1
IO-SELECT-2
IO-SELECT-3
IO-SELECT-4
IO-SELECT-5
IO-SELECT-6
IO-SELECT-7
Peripheral Card ROM Address Space:
I/O Select 1 - C100-C1FF
I/O Select 2 - C200-C2FF
I/O Select 3 - C300-C3FF
I/O Select 4 - C400-C4FF
I/O Select 5 - C500-C5FF
I/O Select 6 - C600-C6FF
I/O Select 7 - C700-C7FF
F13
KBD
CLR_STB
Cassette_Out
SPKR_Out
GamePort_Strobe
PHI0
F14
74LS259
SS-GR_TXT
SS-Mix_NoMix
SS-PG2_PG1
SS-HI_LORES
GamePort_ANN0
GamePort_ANN1
GamePort_ANN2
GamePort_ANN3
SOFT5D
H2
DEV-SEL-0
DEV-SEL-1
DEV-SEL-2
DEV-SEL-3
DEV-SEL-4
DEV-SEL-5
DEV-SEL-6
DEV-SEL-7
Peripheral Card I/O Locations:
Device Select 0 - C080-C08F
Device Select 1 - C090-C09F
Device Select 2 - C0A0-C0AF
Device Select 3 - C0B0-C0BF
Device Select 4 - C0C0-C0CF
Device Select 5 - C0D0-C0DF
Device Select 6 - C0E0-C0EF
Device Select 7 - C0F0-C0FF
H14
74LS251
A[0..15]
D7
H13
NE558
R20
PDL0
100R
Cap8
.022uF
R23
PDL3
Cap7
R22
PDL2
R21
PDL1
Cap5
Cap6
Cap9
.1uF
J0
Cassette Data In
Cap10
R15
1M
R16
12K
R30
R17
R29
K13
MA741
CASSETTE_IN
J14
GAME_IO_Conn
PDL0
PDL2
J13A
74LS74
SPKR_Out
Cap11
R24
47K
CR1
1N914
Q4
MPSA13
R25
27R
Cap12
SPKR1
Speaker Connector
J13B
SOFT5D
Cassette_Out
R19
12K
R18
100R
J2
Cassette Data Out
J13C
Captured from the Apple II Reference Manual (1979)
Sheet: /IO_AddressDecode/
File: IO_AddressDecode.kicad_sch
Title: Apple II+ Schematic
Size: A4
Date:
Rev: 0
KiCad E.D.A. kicad 7.0.10
Id: 9/9